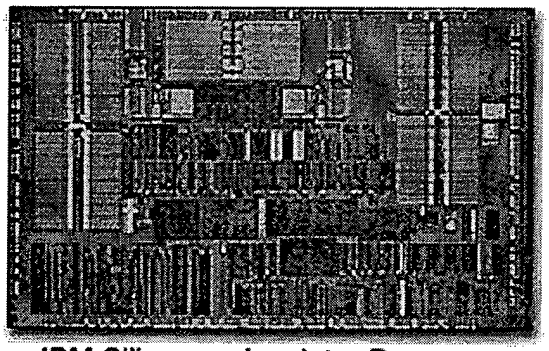
# Silicon-On-Insulator Technology - Page 1/4

*Review Date:* November 8, 2000

*Reviewer:* Robert Richmond

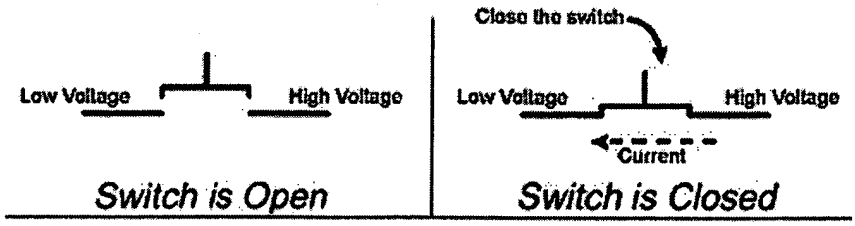


IBM Silicon-on-Insulator Processor

Imagine computer processors scaling to 5,000MHz and beyond within the next four years. Intel hopes to market the advanced NorthWood Pentium IV design, AMD hopes to move desktop users to the K8 Clawhammer, and even upcoming companies like Transmeta and VIA hope to market 3,000MHz+ chips by 2005. The performance offered by these future generation chips will be staggering, but all of these designs suffer a common roadblock. Current semiconductor fabrication techniques are bounded by the physical limitations inherent in silicon gate technology. A new approach offered by IBM, dubbed Silicon-On-Insulator (SOI), is intended to overcome these limitations. SOI offers manufacturers the ability to fabricate higher clocked CPUs while lowering the power demands of these high-performance components.

# Current Technology






The mass proliferation of the transistor in the 1960's provided the catalyst to fuel a computer technology revolution within the semiconductor industry. A transistor is an electronic version of a simple electrical switch, which is illustrated above. A switch has two electrical states, open and closed. An open switch does not bridge the circuit, thus electrical current may not pass through. A closed switch allows conducting of a current, since the bridge is connected. A transistor uses the same approach as any standard switch, but the control gate is switched with an electrical field current.

## Current Technology (cont'd)/CMOS Limitations

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### Silicon-On-Insulator Technology - Map

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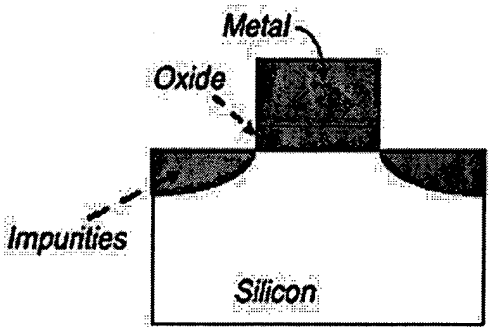
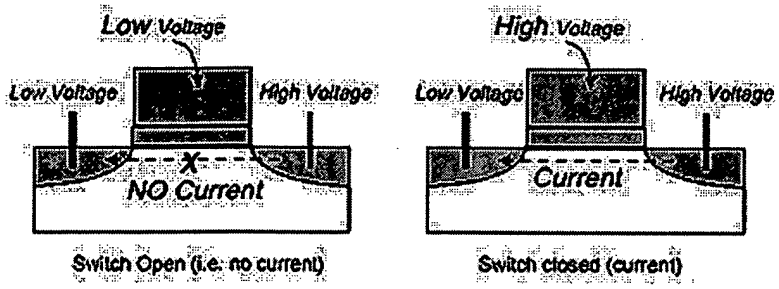
## Current Technology (cont'd)




Current CPU core transistors are based on the metal-oxide semiconductor (MOS) design. As represented in the images above and below, the MOS approach uses a filament of metallic oxide placed on a silicon surface. Pure silicon will not effectively conduct electricity, so impurities (usually a silicon cyanide derivative) are embedded within the substrate to form the conductive paths. When a high-voltage current is passed through the metal layer, the corresponding metal oxide path will allow electricity to pass between the impurity layers. This switching circuit can be regarded as a semi-conductor, as the MOS circuit can become either a conductor or an insulator

with a simple current change.




CMOS is an updated MOS standard that drives most electronic devices found within a computer. Complementary Metal-Oxide Semi-conductor technology operates in the same manner as the MOS method, but the voltage drive is reversed. To complete the circuit within a CMOS device, the voltage applied to the metal conducting layer must be low-voltage in nature in order for the circuit to close. By utilizing both CMOS and MOS circuits, a CPU design can effectively operate at higher speeds since it can operate with alternating voltage states simultaneously. Most computer-related electronic devices are composed of both circuit types, but for simplification, most hardware engineers refer to the technology as just CMOS.

## CMOS Limitations

Current CMOS fabrication techniques will not be viable in upcoming generations of processors. Current CPUs are primarily manufactured using aluminum metal layers within the transistor gate array. These aluminum layers have proven to be ineffective above 1.1GHz. Intel's recent recall of all Pentium III 1.13GHz chips is an indicating factor. The Pentium III core yield rate above 933MHz has been rather poor. The effects are not limited to Intel. AMD's higher-clocked Athlon Thunderbirds are now being manufactured using a copper interconnect process. Copper is a better solution with less resistance and better conductivity than aluminum. Most of AMD's aluminum based CPUs have poor yield rates above 1GHz compared to their copper siblings.

Through computer aided testing, most manufacturers agree that CMOS technology will not be able to scale efficiently below the .10 micron die size. Current CPUs, such as the Pentium III, are manufactured with a .18-micron process. The

need for smaller die sizes is clearly evident as core clock speeds increase. CMOS technology could be outdated quickly with the theoretical practical limit of .10 micron. A new process will be needed to replace this aging standard. The answer to the problem will likely arrive with the introduction of the Silicon-on-Insulator semiconducting fabrication process.

## Silicon-on-Insulator Explained/Fabrication Concerns

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### Silicon-On-Insulator Technology - Map

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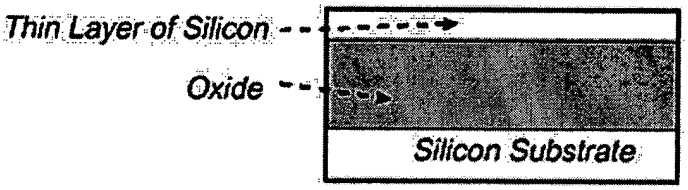
## Silicon-on-Insulator Explained




Silicon-on-Insulator differs from CMOS by placing the transistor's silicon junction area on top of an electrical insulator. The most common insulators employed with this technique are glass and silicon oxide. With the SOI technique, the gate area can be assured of minimal capacitance, which is a measure of ability to store an electrical charge. Any medium that can conduct electricity has some degree of capacitance. Technically, a MOS transistor is regarded as a capacitive circuit. This implies that the MOS circuit must completely charge to full capacitance to activate its switching capability. The process of discharging and recharging the transistor requires a relatively long amount of time in contrast to the time it requires to actually switch the voltage state of the



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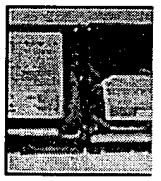

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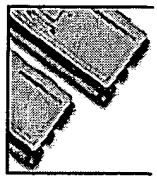

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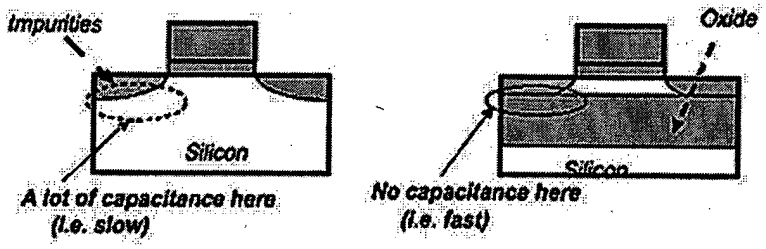
transistor's metal layer. SOI attempts to eliminate this capacitance, as a low capacitance circuit will allow faster transistor operation. As transistor latency drops, the ability to process more instructions in a given time rises.




The diagram above represents a MOS circuit (left) as compared to an SOI circuit (right). The MOS circuit is slower because a capacitance develops between the impurity layers and the silicon substrate. This boundary area is known as the junction capacitance layer. As noted earlier, a MOS circuit must spend a large amount of its operational time discharging and recharging this capacitance. In comparison, the SOI circuit employes silicon oxide layered over the pure silicon substrate. The SOI circuit's capacitance will be negligible since the silicon oxide provides an efficient insulation barrier. The junction capacitance area is eliminated by SOI, thus the transistor will be able to operate faster since the charging process is eliminated.

## Fabrication Concerns

The base silicon substrate found within MOS circuits has a perfect crystalline substructure. The insulator (silicon oxide) layer of the SOI surface lacks a crystalline composition. These differences make production of pure crystal silicon difficult when bonded with the non-crystal oxide insulator. The same applies even if glass is used, as the crystalline nature of pure silicon creates difficulties in bonding it to any other material.

In the 1990's IBM's microelectronics research division tried adapting SOI technology for alternative insulating materials. The most promising substance found was sapphire, but it proved to be flawed as well. Extensive research found that sapphire would deteriorate quite easily. Early fabrication

testing at IBM's Advanced Silicon Technology Center indicated yield rates would prove unsatisfactory for production level marketing of a silicon-on-sapphire based CPU.

## SIMOX/Real-World Performance/Conclusion

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### Silicon-On-Insulator Technology - Map



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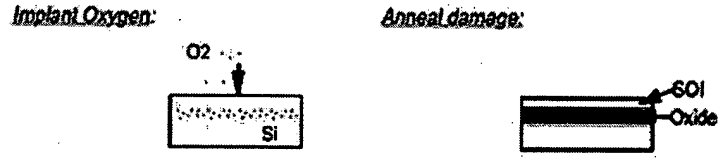
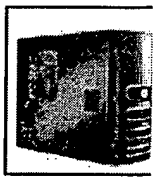
## SIMOX




However, IBM did succeed with another Silicon-on-Insulator project. IBM has found a way to overcome the inherent problems associated with mating pure crystal silicon with a non-crystal insulator. Separation by Implantation of Oxygen (SIMOX) is a radically new fabrication technique. SIMOX works by creating a perfectly smooth .15-micron layer of silicon oxide SOI film. This new SOI film features virtually no imperfections or impurities while retaining high yield rates. The SIMOX process involves direct injection of purified oxygen into a silicon wafer at extremely high temperatures. Under the high temperature, oxygen bonds with the silicon, forming the thin layers of silicon oxide film. This relatively perfect silicon oxide allows direct bonding to the pure crystalline silicon substrate.





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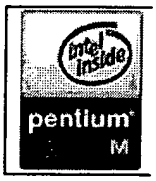


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After the film is harvested, it can be incorporated into a MOS circuit with only minor alterations to the CMOS production process. In fact, the same lithography techniques, tool sets, and metal bonding processes are involved. Through relatively minor restructuring of current fabrication foundries, even Intel or AMD could produce SOI based chips. IBM is currently field testing the SIMOX technique, and the results look promising. The current validated production die size for SOI chips is .22 micron, but IBM plans to aggressively move toward a .15-micron process in the near future.



## Real-World Performance

IBM laboratory testing shows SOI based processors feature a 20-25% improvement in transistor cycle time compared to similar CMOS engineered chips. Performance gains are averaging 25-35% when SOI is employed. Silicon-on-Insulator has also proven to be useful for low power situations. SOI manufactured processors require an average of 40-50% less power than their CMOS counterparts.

Another key benefit of SOI is a reduction in soft error rates. Soft errors refer to data corruption caused by cosmic rays and natural radioactive background signals. SER will be an important issue as CPUs scale to smaller die sizes and lower voltages. Silicon-on-Insulator chips indicate a significant reduction in SER related issues, even with current large die chips.

## Conclusion

Silicon-on-Insulator is shaping up to be an evolutionary step in CPU manufacturing. IBM hopes to develop and market 5GHz+ processors within the next four to five years. AMD has already expressed interest, as SOI could allow the next generation 64-bit K8 architecture to scale well beyond original expectations. Samsung is another interested party; with its upcoming 64-bit 21264E licensed Compaq Alpha derivative rumored to be an SOI solution. Current press releases indicate the .18-micron 21264E processor is already reaching 1.2GHz with excellent yield rates. This level of performance is impressive, as the Alpha architecture is a complex design and the Samsung alternative is still a

pre-production chip.

Silicon-on-Insulator is an exciting technology. The reduced capacitance SOI will likely usher in a new era of high-performance computing. Other exciting features include decreased power dissipation and improvements in soft error related issues. Industry analysts predict Silicon-on-Insulator technology should start to appear in consumer-oriented devices around early 2002. That 5,000MHz+ system might be closer than anyone imagined!

## Silicon-On-Insulator Technology - Map



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